programmable transistors in the substrate of said programmable interconnect chip; and

means for programming said programmable transistors in said interconnect chip so as to turn on selected ones of the transistors in said programmable interconnect chip to form desired interconnections between selected contacts on said printed circuit board.--

Add new Claims 23 - 77 as given below:

--23. Structure comprising a printed circuit board and a programmable interconnect chip for programmably interconnecting electronic components formed on said printed circuit board, said chip comprising:

a substrate;

a first set of conductive leads formed across said substrate in a first direction;

a second set of conductive leads formed across said substrate in a second direction not parallel to said first direction, portions of selected ones of said conductive leads in at least one of said first and second sets of conductive leads being connected to pads on the surface of said chip, each pad being adapted for contact to a corresponding contact on said printed circuit board, at least one conductive lead in at least one of said first and second sets of conductive leads comprising two or more electrically separate conductive segments; and

means for programmably interconnecting selected ones of said conductive leads or segments, thereby to enable said electronic components to be programmably interconnected.

24. Structure as in Claim 23 wherein said pads are arranged in an area matrix of rows and columns such that at least one of said pads is internal to the pads along the periphery of said area matrix.

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6 25. Structure as in Claim 5 wherein:

said first set of conductive leads comprises a first plurality of first groups of conductive leads, each first group of conductive leads being located adjacent to a selected row of said pads; and

said second set of conductive leads comprises a second plurality of second groups of conductive leads, each second group of conductive leads being located adjacent to a selected column of said pads.

7 26. Structure as in Claim 5 wherein:

said first set of conductive leads comprises a first plurality of groups of rows of conductive leads, each of at least two of said groups of rows of conductive leads being located between two adjacent rows of said pads; and

said second set of conductive leads comprises a second plurality of groups of columns of conductive leads, each of at least two of said groups of columns of conductive leads being located between two adjacent columns of said pads.

8 27. Structure as in Claim 4 wherein said means for programmably interconnecting comprises:

a plurality of programming transistors;

means for electrically connecting selected ones of said conductive leads or segments to said programming transistors; and

means for selectively activating said programming transistors so as to form interconnections between selected ones of said conductive leads or segments.

9 28. Structure as in Claim 4 wherein said means for programmably interconnecting further includes a plurality of interconnect structures, each comprising:

a first conductive layer comprising a portion of one

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of said conductive leads or segments in said first set of conductive leads;

a second conductive layer comprising a portion of one of said conductive leads or segments in said second set of conductive leads; and

dielectric material between said first and second layers, said dielectric material being capable of being made conductive by the application of a selected voltage thereto so as to form an electrically conductive path between said first and second layers.

29. Structure comprising:

a board suitable for carrying electrically conductive traces;

a plurality of component contacts formed on said board for receipt of electronic components;

a plurality of electrically conductive traces formed on said board, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

at least one programmable integrated circuit connected to said board and containing a plurality of electrically conductive leads, each of said conductive leads being electrically connected to a corresponding one of said conductive traces on said board thereby to form an electrically conductive path from each component contact to the corresponding conductive lead, said at least one programmable integrated circuit being programmable by a user through said conductive leads to selectively interconnect said conductive traces on said board to achieve a desired electrical function from the electronic components to be connected to said board; and

at least one bus for transmitting information between a computer and said at least one programmable integrated circuit.

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30. Structure as in Claim 29 wherein said component contacts and said conductive traces on said board have a standard configuration independent of the electronic components to be connected to said board and the electrical function to be implemented by said electronic components when selectively interconnected by said at least one programmable integrated circuit.

31. Structure as in Claim 29 wherein said board contains more than one layer of said conductive traces.

32. Structure as in Claim 29 wherein said at least one bus transmits information for exercising circuitry on said board.

33. Structure as in Claim 29 wherein said at least one bus transmits information for testing circuitry on said board.

34. Structure as in Claim 29 wherein said at least one bus transmits information for programming said at least one programmable integrated circuit.

35. Structure as in Claim 34 wherein said at least one bus transmits information for exercising circuitry on said board, thereby allowing said circuitry to be exercised during programming of said at least one programmable integrated circuit.

36. Structure as in Claim 34 wherein said at least one bus transmits information for testing circuitry on said board, thereby allowing said circuitry to be tested during programming of said at least one programmable integrated circuit.

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37. Structure comprising:

a board suitable for carrying electrically conductive traces;

a plurality of component contacts formed on said board for receipt of electronic components;

a plurality of electrically conductive traces formed on said board, each of said conductive traces being electrically connected to a corresponding one of said component contacts; and

at least one programmable integrated circuit connected to said board, each programmable integrated circuit comprising:

a substrate;

a first set of electrically conductive leads formed across said substrate in a first direction;

a second set of electrically conductive leads formed across said substrate in a second direction not parallel to said first direction, at least one conductive lead in at least one of said first and second sets of conductive leads being divided into at least two electrically separate conductive segments; and

means for programmably interconnecting selected ones of said conductive leads or segments;

wherein each of a selected number of said conductive leads of said at least one programmable integrated circuit is electrically connected to a corresponding one of said conductive traces on said board thereby to form an electrically conductive path from each component contact to the corresponding conductive lead; and

wherein said at least one programmable integrated circuit is programmable by a user through said conductive leads to selectively interconnect said conductive traces on said board to achieve a desired electrical function from the electronic components to be connected to said board.

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38. Structure as in Claim 37 wherein said board contains more than one layer of said conductive traces.

39. Structure as in Claim 37 further including at least one bus for transmitting information between a computer and said at least one programmable integrated circuit.

40. Structure comprising:

a substrate;

a plurality of component contacts formed on said substrate for receipt of electronic components;

a plurality of electrically conductive traces formed on said substrate, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

at least one programmable integrated circuit connected to said substrate and containing a plurality of electrically conductive leads, said at least one programmable integrated circuit being programmable by a user through said conductive leads to selectively interconnect said conductive traces on said substrate to achieve a desired electrical function from the electronic components to be connected to said substrate;

wherein each of said conductive leads of said at least one programmable integrated circuit is electrically connected to a corresponding one of said conductive traces on said substrate thereby to form an electrically conductive path from each component contact to the corresponding conductive lead; and

wherein said component contacts and said conductive traces on said substrate have a standard configuration independent of the electronic components to be mounted on said substrate and the electrical function to be implemented by said electronic components when selectively interconnected by said at least one programmable integrated circuit.

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41. Structure in Claim 43 wherein said substrate contains more than one layer of said conductive traces.

42. Structure comprising:

a main substrate;

a plurality of component contacts formed on said main substrate for receipt of electronic components;

a plurality of electrically conductive traces formed on said main substrate, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

at least one programmable integrated circuit connected to said main substrate, each programmable integrated circuit comprising:

a chip substrate;

a first set of electrically conductive leads formed across said chip substrate in a first direction;

a second set of electrically conductive leads formed across said chip substrate in a second direction not parallel to said first direction, at least one conductive lead in at least one of said first and second sets of conductive leads being divided into at least two electrically separate conductive segments; and

means for programmably interconnecting selected ones of said conductive leads or segments;

wherein each of a selected number of said conductive leads of said at least one programmable integrated circuit is electrically connected to a corresponding one of said conductive traces on said main substrate thereby to form an electrically conductive path from each component contact to the corresponding conductive lead; and

wherein said at least one programmable integrated circuit is programmable by a user through said conductive leads to selectively interconnect said conductive traces on said main substrate to achieve a

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desired electrical function from the electronic components to be connected to said main substrate.

43. A method comprising the steps of:

providing input signals from a computer to at least one programmable integrated circuit which (a) is connected to a substrate, (b) contains a plurality of electrically conductive leads each connected by way of a corresponding one of a plurality of electrically conductive traces formed on said substrate to a corresponding one of a plurality of component contacts formed on said substrate for receipt of electronic components, and (c) is programmable for selectively interconnecting said conductive leads in order to programmably interconnect said electronic components to achieve a desired electrical function; and

providing output signals from said at least one programmable integrated circuit to said computer.

44. A method as in Claim 43 wherein said component contacts and said conductive traces on said substrate are arranged in a standard configuration independent of said electronic components.

45. A method as in Claim 43 wherein said input and output signals carry information for exercising circuitry on said substrate.

46. A method as in Claim 43 wherein said input and output signals comprise test signals for testing circuitry on said substrate.

47. A method as in Claim 43 wherein said input and output signals comprise programming signals for controlling the selective interconnection of said conductive leads of said at

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least programmable integrated circuit during programming of said at least programmable integrated circuit.

48. A method as in Claim 47 wherein said input and output signals include test signals for testing circuitry on said substrate.

49. A method as in Claim 43 wherein said substrate comprises a board suitable for carrying electrically conductive traces.

50. A method comprising the steps of:

providing input signals from a computer to at least one programmable integrated circuit which (a) is connected to a substrate, (b) contains a first set of electrically conductive leads extending in a first direction and a second set of electrically conductive leads extending in a second direction different from said first direction where at least one conductive lead in at least one of said sets of conductive leads is divided into at least two electrically separate conductive segments and where each of a selected number of said conductive leads is connected to a corresponding one of a plurality of component contacts formed on said substrate for receipt of electronic components, and (c) is programmable for selectively interconnecting said conductive leads in order to programmably interconnect said electronic components to achieve a desired electrical function; and

providing output signals from said at least one programmable integrated circuit to said computer.

51. A method as in Claim 50 wherein said input and output signals carry information for exercising circuitry on said substrate.

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52. A method as in Claim 50 wherein said input and output signals comprise (a) test signals for testing circuitry on said substrate and/or (b) programming signals for controlling the selective interconnection of said conductive leads of said at least one programmable integrated circuit.

53. A method comprising the steps of:

providing programming signals from a computer to at least one programmable integrated circuit connected to a substrate for controlling selective interconnection of a plurality of electrically conductive leads of said at least one programmable integrated circuit, each of said conductive leads being connected by way of a corresponding one of a plurality of electrically conductive traces formed on said substrate to a corresponding one of a plurality of component contacts formed on said substrate for receipt of electronic components such that the electronic components are programmably interconnected to achieve a desired electrical function; and

furnishing test signals from said computer to said at least one programmable integrated circuit to test circuitry on said substrate.

54. A method as in Claim 53 further including the step of furnishing status signals from said at least one programmable integrated circuit to said computer.

55. A method as in Claim 54 further including the step of controllably activating buffer circuitry contained in said at least one programmable integrated circuit to allow either said test signals or said status signals to pass through said buffer circuitry.

56. A method as in Claim 53 wherein said substrate comprises a board suitable for carrying electrically conductive

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traces.

57. Structure comprising:

a board suitable for carrying electrically conductive traces;

a plurality of component contacts formed on said board for receipt of electronic components;

a plurality of electrically conductive traces formed on said board, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

at least one programmable integrated circuit connected to said board and containing a plurality of electrically conductive leads, each of said conductive leads being electrically connected to a corresponding one of said conductive traces on said board thereby to form an electrically conductive path from each component contact to the corresponding conductive lead, said at least one programmable integrated circuit being programmable by a user through said conductive leads to selectively interconnect said conductive traces on said board to achieve a desired electrical function from the electronic components to be connected to said board; and

at least one bus for transmitting information between a computer and circuitry on said board.

58. Structure as in Claim 57 wherein said component contacts and said conductive traces on said board have a standard configuration independent of the electronic components to be connected to said board and the electrical function to be implemented by said electronic components when selectively interconnected by said at least one programmable integrated circuit.

59. Structure as in Claim 57 wherein said board contains more than one layer of said conductive traces.

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60. Structure as in Claim 57 wherein said at least one bus transmits information for exercising circuitry on said board.

61. Structure as in Claim 57 wherein said at least one bus transmits information for testing circuitry on said board.

62. Structure as in Claim 57 wherein said at least one bus transmits information for programming said at least one programmable integrated circuit.

63. Structure as in Claim 62 wherein said at least one bus transmits information for exercising circuitry on said board, thereby allowing said circuitry to be exercised during programming of said at least one programmable integrated circuit.

64. Structure as in Claim 62 wherein said at least one bus transmits information for testing circuitry on said board, thereby allowing said circuitry to be tested during programming of said at least one programmable integrated circuit.

65. A method comprising the steps of:

providing input signals from a computer to circuitry on a substrate connected to at least one programmable integrated circuit which (a) contains a plurality of electrically conductive leads each connected by way of a corresponding one of a plurality of electrically conductive traces formed on said substrate to a corresponding one of a plurality of component contacts provided on said substrate for receiving electronic components and (b) is programmable for selectively interconnecting said conductive leads in order to programmably interconnect said electronic components to achieve a desired electrical function; and

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providing output signals from circuitry on said substrate to said computer.

66. A method as in Claim 65 wherein said component contacts and said conductive traces on said substrate are arranged in a standard configuration independent of said electronic components.

67. A method as in Claim 65 wherein said input and output signals carry information for exercising circuitry on said substrate.

68. A method as in Claim 65 wherein said input and output signals comprise test signals for testing circuitry on said substrate.

69. A method as in Claim 65 wherein said input and output signals comprise programming signals for controlling the selective interconnection of said conductive leads of said at least programmable integrated circuit during programming of said at least programmable integrated circuit.

70. A method as in Claim 69 wherein said input and output signals include test signals for testing circuitry on said substrate.

71. A method as in Claim 65 wherein said substrate comprises a board suitable for carrying electrically conductive traces.

72. Structure comprising:

at least one substrate;

a plurality of component contacts formed on said at least one substrate for receipt of electronic components;

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a plurality of electrically conductive traces formed on said at least one substrate, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

a group of programmable integrated circuits connected to said at least one substrate, each programmable integrated circuit containing a plurality of electrically conductive leads capable of being programmably interconnected by a user, each of a selected number of said conductive leads being electrically connected to a corresponding one of said conductive traces on said at least one substrate thereby to form an electrically conductive path from each component contact to the corresponding conductive lead; and

a bus system for electrically interconnecting said programmable integrated circuits, said bus system being connected to selected ones of said conductive leads, whereby said conductive traces and said bus system can be programmably interconnected through said programmable integrated circuits to achieve a desired electrical function from the electrical components to be connected to said at least one substrate.

18 73. Structure as in Claim 17 wherein at least one of said at least one substrate contains more than one layer of said conductive traces.

19 74. Structure as in Claim 17 wherein said bus system comprises electrically conductive traces formed on at least one of said at least one substrate.

20 75. Structure as in Claim 17 wherein said bus system comprises a central bus and a group of further busses, each further bus electrically connecting the central bus to a corresponding one of said programmable integrated circuits.

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21 76. Structure as in Claim 72 wherein:

the central bus comprises a first layer of electrically conductive traces formed on one of said at least one substrate; and

at least one of the further busses comprises a second layer of electrically conductive traces formed on said one of said at least one substrate and spaced vertically apart from said first layer of conductive traces.

22 77. Structure as in Claim 76 wherein said one of said at least one substrate has holes containing electrically conductive material that electrically connects said first layer of conductive traces to said second layer of conductive traces.--

REMARKS

Aside from the priority information, the specification has been amended in the same way as in parent U.S. patent application Ser. No. 08/171,992. These revisions include the changes to identify new Fig. 9 which is being added just as in the parent application and in the grandparent application, Ser. No. 07/410,194.

The claims have been revised to carry over the claims that were pending, but not allowed, in the parent application. In particular, new Claims 23 - 39 respectively repeat the like-numbered claims of the parent application. Claims 40 - 77 respectively repeat Claims 43 - 74 and 80 - 85 of the parent application.

The application is now in a condition suitable for

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